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# 4H-SiC MIS Capacitors and MISFETs With Deposited $\text{SiN}_x/\text{SiO}_2$ Stack-Gate Structures

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**Abstract**— $\text{SiN}_x/\text{SiO}_2$  stack-gate structures, followed by  $\text{N}_2\text{O}$  annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–voltage measurements on fabricated stack-gate MIS capacitors have indicated that the interface trap density is reduced by post-deposition annealing in  $\text{N}_2\text{O}$  at  $1300^\circ\text{C}$ . When the MIS capacitor with a  $\text{SiN}_x/\text{SiO}_2$  thickness of 10 nm/50 nm was annealed in  $\text{N}_2\text{O}$  for 2 h, the interface trap density at  $E_C - 0.2\text{ eV}$  is below  $1 \times 10^{11}\text{ cm}^{-2}\text{eV}^{-1}$ . Oxidation of  $\text{SiN}_x$  during  $\text{N}_2\text{O}$  annealing has resulted in the improvement of SiC MIS interface characteristics, as well as dielectric properties. The fabricated MISFETs with  $\text{SiN}_x/\text{SiO}_2$  stack-gate structure annealed in  $\text{N}_2\text{O}$  demonstrate a reasonably high channel mobility of  $32\text{ cm}^2/\text{V} \cdot \text{s}$  on the (0001)Si face and  $40\text{ cm}^2/\text{V} \cdot \text{s}$  on the (0001)C face.

**Index Terms**—Channel mobility, deposited insulator, interface trap density, metal–insulator–semiconductor (MIS), MOSFET, silicon carbide (SiC), silicon nitride ( $\text{SiN}_x$ ), silicon oxynitride ( $\text{SiO}_x\text{N}_y$ ).

## I. INTRODUCTION

SILICON carbide (SiC) is an attractive wide-band-gap semiconductor that has superior properties, such as high breakdown field, high thermal conductivity, and high saturation electron drift velocity [1]. Among many SiC polytypes, 4H-SiC is the polytype suitable for high-power devices in the next generation due to its high bulk mobility and its small anisotropy. Recent progress in SiC growth and device technology has led to the commercial release of high-voltage 4H-SiC Schottky rectifiers [2], [3], and SiC MOSFETs have been regarded as a promising candidate for low-loss and fast power devices in advanced electronic systems [4].

Although 4H-SiC MOSFETs have great potential for high-power switches, the fabricated MOSFETs with thermal oxide grown in dry  $\text{O}_2$  ambient exhibit a low channel mobility below  $10\text{ cm}^2/\text{V} \cdot \text{s}$  because of its high  $\text{SiO}_2/\text{SiC}$  interface trap density. In order to overcome this problem, various methods have been investigated. For example, wet reoxidation or “nitridation” of the SiC MOS interface [5]–[8] and the usage of

4H-SiC (000 $\bar{1}$ ) or (11 $\bar{2}0$ ) face [9], [10] are effective processes to increase the channel mobility of SiC MOSFETs. These investigations on SiC MOS technology have mainly focused on thermal oxide. However, the interfacial transition layer, which contains carbon atoms or carbon cluster in the  $\text{SiO}_2$ , is detected between pure  $\text{SiO}_2$  grown by thermal oxidation and SiC [11], [12]. Although the origin of interface traps has not fully been understood, the thickness of interfacial transition layer is correlated with the channel mobility. (The thick transition layer at the  $\text{SiO}_2/\text{SiC}$  interface may reduce the channel mobility [12].) On the other hand, the transition layer at the interface will hardly be formed when the gate insulator is deposited. Therefore, the deposited insulator/SiC interface may be abrupt and can be expected to show better characteristics than the thermal oxide/SiC interface. The deposited insulators also have other advantages: 1) superior reliability (when adequately processed) [13]; 2) reduction of process time; and 3) isotropic formation of oxide on the trench sidewalls. From these advantages, deposited insulators are one of the attractive candidates for the gate insulators of SiC metal–insulator–semiconductor (MIS) devices.

A few groups have started to investigate SiC MOS structures with deposited insulator [14]–[16]. SiC MOSFETs with deposited  $\text{SiO}_2$  followed by  $\text{N}_2\text{O}$  annealing [17] and low-temperature deposited  $\text{Al}_2\text{O}_3$  [18] have already demonstrated a higher channel mobility than the MOSFETs with thermal oxide. In this paper, the authors adopt  $\text{SiN}_x/\text{SiO}_2$  stack-gate structures deposited by plasma-enhanced chemical vapor deposition (PECVD), followed by  $\text{N}_2\text{O}$  annealing. In the proposed structure, by inserting other dielectrics between SiC and  $\text{SiO}_2$ , an adverse impact of near-interface traps located at  $E_C - 2.77\text{ eV}$  in  $\text{SiO}_2$  [19] may be minimized. In addition, the deposited insulator may suppress the formation of the interfacial transition layer, as previously mentioned. The authors have succeeded in reducing the density of interface traps and enhancing the channel mobility, compared to  $\text{N}_2\text{O}$  oxidation, in SiC MISFETs fabricated with a deposited  $\text{SiN}_x/\text{SiO}_2$  stack-gate structure annealed in  $\text{N}_2\text{O}$ .

## II. DEVICE FABRICATION

For the fabrication of MIS capacitors, n-type 4H-SiC (0001) epilayers with a donor concentration of  $1 \times 10^{16}\text{ cm}^{-3}$ , purchased from Cree, were prepared. The gate formation procedure used in this study is shown in Fig. 1. Fig. 1(a) and (b) shows the process to form  $\text{SiN}_x/\text{SiO}_2$  stack-gate structures. After RCA cleaning with final hydrofluoric acid dip, the  $\text{SiN}_x$  layer was deposited by PECVD with  $\text{SiH}_4$  and  $\text{NH}_3$  as source gases. The thickness of deposited  $\text{SiN}_x$  was varied from

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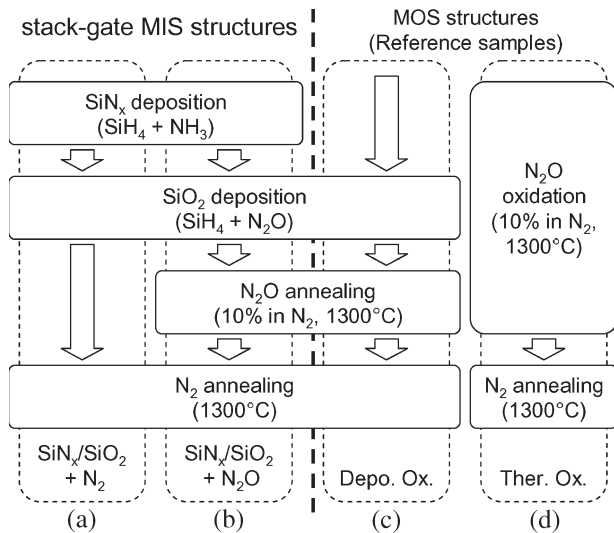


Fig. 1. Experimental procedure for stack-gate MIS structures annealed in (a)  $\text{N}_2$  and (b)  $\text{N}_2\text{O}$  and MOS structures with (c) deposited oxide and (d) thermal oxide. MOS structures with oxide (without  $\text{SiN}_x$  layer) were fabricated as a reference.

2 to 10 nm. Then, subsequent  $\text{SiO}_2$  deposition was carried out. In the  $\text{SiO}_2$  deposition,  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  were used as source gases. The deposited thickness of  $\text{SiO}_2$  was about 50 nm. The typical deposition temperature of  $\text{SiN}_x$  and  $\text{SiO}_2$  was 400 °C. After the PECVD process, thermal annealing was performed in dry  $\text{N}_2\text{O}$  (10% diluted in  $\text{N}_2$ ) and  $\text{N}_2$  ambient at 1300 °C.  $\text{N}_2\text{O}$ -annealing time was varied, ranging from 30 min to 2 h [Fig. 1(b)]. During  $\text{N}_2\text{O}$  annealing, a portion of the  $\text{SiN}_x$  layer was oxidized and converted to the  $\text{SiO}_x\text{N}_y$  layer. Some of the samples were not annealed in  $\text{N}_2\text{O}$  [Fig. 1(a)]. MOS structures deposited by PECVD, with  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  as source gases [Fig. 1(c)], and formed by direct oxidation of SiC in dry  $\text{N}_2\text{O}$  (10% diluted in  $\text{N}_2$ ) ambient at 1300 °C [Fig. 1(d)] [12] were also prepared as a reference. The reference samples have a  $\text{SiO}_2/\text{SiC}$  interface (without the  $\text{SiN}_x$  layer). The equivalent oxide thickness (EOT) calculated from the accumulation capacitance was about 60 nm. Al was evaporated on the backside and annealed at 600 °C for 10 min. The circular gate metal was Al, with a diameter of 520  $\mu\text{m}$  for capacitance–voltage ( $C$ – $V$ ) measurements and 180  $\mu\text{m}$  for current–voltage ( $I$ – $V$ ) measurements.

The authors have also fabricated n-channel MISFETs on p-type 4H-SiC (0001) epilayers with an acceptor concentration of  $8 \times 10^{15} \text{ cm}^{-3}$  and on p-type 4H-SiC (000 $\bar{1}$ ) epilayers with an acceptor concentration of  $6 \times 10^{15} \text{ cm}^{-3}$ , purchased from Cree. The source–drain regions were formed by high-dose ( $5 \times 10^{15} \text{ cm}^{-2}$ )  $\text{P}^+$  implantation at 300 °C. After ion implantation, high-temperature annealing was performed at 1600 °C for 15 min in Ar with a carbon cap to suppress surface roughening [21]. The formation of gate insulators was the same process as that previously mentioned. Ti/Al and Al annealed at 600 °C for 10 min were used as the backside and source–drain contacts, respectively. The gate metal was Al. The typical channel length  $L$  and width  $W$  were in the range of 25–100  $\mu\text{m}$  and 200  $\mu\text{m}$ , respectively. In order to estimate exact channel mobility and suppress short-channel effects [20], the authors adopted the design of long-channel lateral MOSFETs.

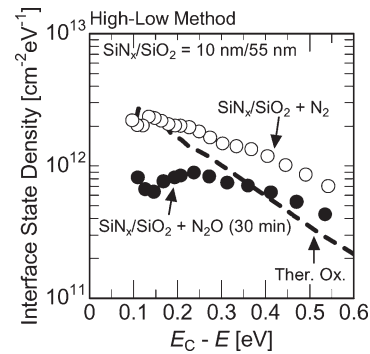


Fig. 2. Interface trap density of the  $\text{SiN}_x/\text{SiO}_2$  stack-gate MIS capacitor annealed in  $\text{N}_2$  and  $\text{N}_2\text{O}$ . The open and closed circles denote the MIS capacitors annealed in  $\text{N}_2$  and  $\text{N}_2\text{O}$ , respectively. The  $\text{SiN}_x/\text{SiO}_2$  stack-gate structure is 10 nm/55 nm. The dashed line represents the MOS capacitor with thermal oxide.

### III. EXPERIMENTAL RESULT AND DISCUSSION

Quasi-static and high-frequency (1 MHz)  $C$ – $V$  characteristics ( $C_{\text{QS}}$  and  $C_{\text{HF}}$ , respectively) were measured by using a simultaneous  $C$ – $V$  system at room temperature under dark conditions. From the  $C$ – $V$  curves, interface trap density was calculated by a high–low method.

The density of interface traps determined by a high–low method for stack-gate MIS capacitors with a deposited  $\text{SiN}_x/\text{SiO}_2$  thickness of 10 nm/55 nm is represented in Fig. 2. The stack-gate MIS capacitors were annealed in  $\text{N}_2$  or  $\text{N}_2\text{O}$  ambient for 30 min. Fig. 2 also shows the interface trap density for a MOS capacitor with thermal oxide grown in the  $\text{N}_2\text{O}$  ambient (“Ther. Ox.”). The density of interface traps for the stack-gate MIS capacitor annealed in  $\text{N}_2\text{O}$  (“ $\text{SiN}_x/\text{SiO}_2 + \text{N}_2\text{O}$  (30 min)”) is lower than that for the stack-gate MIS capacitor annealed in  $\text{N}_2$  (“ $\text{SiN}_x/\text{SiO}_2 + \text{N}_2$ ”).  $\text{N}_2\text{O}$  annealing is more effective in reducing the interface trap than  $\text{N}_2$  annealing for the  $\text{SiN}_x/\text{SiO}_2$  stack-gate structure. Compared with thermal oxide, the stack-gate structure, followed by  $\text{N}_2\text{O}$  annealing, exhibits low interface trap density near the conduction band edge. The high density of the interface trap in the shallow energy region causes electron trapping, leading to low channel mobility in 4H-SiC MOSFETs [22].

Fig. 3 shows the results of the secondary ion mass spectrometry measurement for the stack-gate MIS capacitor, followed by  $\text{N}_2\text{O}$  annealing for 30 min (the same device as “ $\text{SiN}_x/\text{SiO}_2 + \text{N}_2\text{O}$  (30 min)”) shown in Fig. 2). The depth profiles of Si, C, N, and O atoms were measured. The depth resolution was about 3 nm. From Fig. 3, the oxygen atoms are clearly detected even between  $\text{SiO}_2$  and SiC, indicating that the initial- $\text{SiN}_x$  layer was oxidized during  $\text{N}_2\text{O}$  annealing. Nitrogen atoms are accumulated at the SiC/ $\text{SiN}_x$  interface, and the concentration of nitrogen atoms at the interface is about  $1 \times 10^{22} \text{ cm}^{-3}$ .

The  $C$ – $V$  characteristics of stack-gate MIS capacitors annealed in  $\text{N}_2\text{O}$  ambient for (a) 30 min and (b) 2 h with a deposited  $\text{SiN}_x/\text{SiO}_2$  thickness of 10 nm/50 nm are represented in Fig. 4. The accumulation capacitance was reduced by increasing the  $\text{N}_2\text{O}$ -annealing time, which means that the  $\text{SiN}_x$  layer is oxidized during  $\text{N}_2\text{O}$  annealing and becomes an  $\text{SiO}_x\text{N}_y$  layer, as shown in Fig. 3. The MIS capacitor annealed

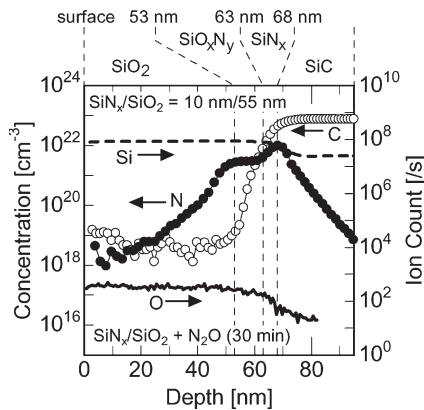


Fig. 3. Results of SIMS measurement for the stack-gate MIS capacitor with a  $\text{SiN}_x/\text{SiO}_2$  thickness of 10 nm/55 nm annealed in  $\text{N}_2\text{O}$  for 30 min. The open and closed circles mean the concentration of carbon and nitrogen atoms, respectively. The dashed line denotes silicon-ion counts, and the solid line denotes oxygen-ion counts.

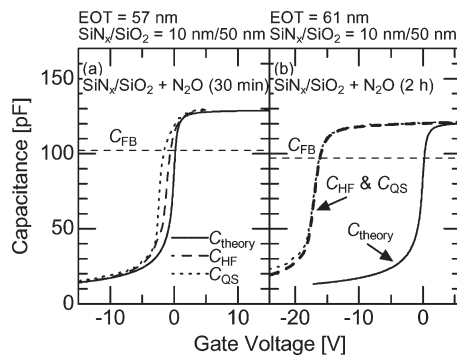


Fig. 4. High-frequency ( $C_{\text{HF}}$ ) and quasi-static ( $C_{\text{QS}}$ )  $C$ - $V$  curves for the  $\text{SiN}_x/\text{SiO}_2$  stack-gate MIS capacitors annealed in  $\text{N}_2\text{O}$  for (a) 30 min and (b) 2 h. The thickness of the  $\text{SiN}_x/\text{SiO}_2$  stack structure is 10 nm/55 nm. The theoretical  $C$ - $V$  curve ( $C_{\text{theory}}$ ) is also shown.

for 30 min shows a small difference between quasi-static and HF  $C$ - $V$  curves. On the other hand, in the MIS capacitor annealed for 2 h, the high-frequency  $C$ - $V$  curve is exactly similar to the quasi-static  $C$ - $V$  curve [Fig. 4(b)], although a large negative flat-band voltage shift (about  $-15$  V) is observed. The effective fixed charge density at the MIS interface of the stack-gate MIS capacitor annealed in  $\text{N}_2\text{O}$  for 30 min and 2 h is about  $2 \times 10^{11} \text{ cm}^{-2}$  (positive) and  $6 \times 10^{12} \text{ cm}^{-2}$  (positive), respectively. The stack-gate MIS capacitor, followed by  $\text{N}_2\text{O}$  annealing for 2 h, exhibits significant increase of effective fixed charge. Fig. 5 represents the interface trap density of stack-gate MIS capacitors annealed in  $\text{N}_2\text{O}$  for 30 min, 1 h, and 2 h (open circles, open squares, and closed circles, respectively, in Fig. 5), demonstrating that the interface trap density could significantly be reduced by extending the  $\text{N}_2\text{O}$ -annealing time. The stack-gate MIS capacitors, followed by  $\text{N}_2\text{O}$  annealing for 30 min and 1 h, show a slight decrease of interface trap density at the shallow energy region from the conduction band edge. The interface trap density of the stack-gate MIS capacitor annealed for 2 h is lower than that of thermal oxide at any energy levels investigated in this study, which are as low as  $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  or below.

The  $I$ - $V$  measurement was also performed. Fig. 6 shows the typical current density-electric field characteristics for the

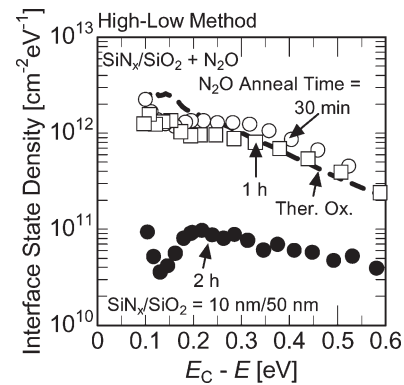


Fig. 5. Interface trap density of the  $\text{SiN}_x/\text{SiO}_2$  stack-gate MIS capacitor annealed in  $\text{N}_2\text{O}$ . The open circles, open squares, and closed circles denote the MIS capacitors annealed for 30 min, 1 h, and 2 h, respectively. The  $\text{SiN}_x/\text{SiO}_2$  stack-gate structure is 10 nm/50 nm. The dashed line corresponds to the MOS capacitor with thermal oxide.

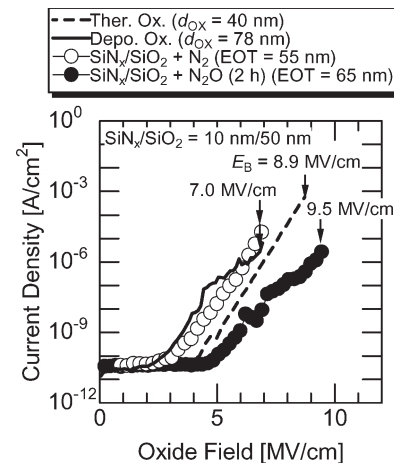


Fig. 6. Current density-electric field characteristics for the stack-gate MIS capacitors and MOS capacitors. The closed and open circles mean the characteristics of the stack-gate MIS capacitors annealed in  $\text{N}_2$  and  $\text{N}_2\text{O}$ , respectively. The stack-gate structures have a  $\text{SiN}_x/\text{SiO}_2$  thickness of 10 nm/50 nm. The dashed and solid lines denote the current density of MOS capacitors with thermal oxide and deposited oxide, respectively.

fabricated stack-gate MIS capacitors and MOS capacitors. The stack-gate MIS capacitors shown in Fig. 6 have a deposited  $\text{SiN}_x/\text{SiO}_2$  thickness of 10 nm/50 nm. The oxide field was corrected by taking account of the flat-band-shift voltage. The typical ramp rate for  $I$ - $V$  measurements was about 0.05 V/s. The gate current was drastically increased, leading to oxide breakdown, after the last point plotted in Fig. 6. The stack-gate MIS capacitor, followed by  $\text{N}_2$  annealing (" $\text{SiN}_x/\text{SiO}_2 + \text{N}_2$ "), and the MOS capacitor with deposited oxide ("Depo. Ox.") show a low breakdown field of about 7 MV/cm. On the other hand, the thermal oxide ("Ther. Ox.") and stack-gate structure, followed by  $\text{N}_2\text{O}$  annealing (" $\text{SiN}_x/\text{SiO}_2 + \text{N}_2\text{O}$ "), exhibit higher breakdown field than other samples. The stack-gate MIS capacitor annealed in  $\text{N}_2\text{O}$  for 2 h demonstrates low leakage current and high breakdown field. It has been reported that deposited insulators, such as ONO stack films formed by chemical vapor deposition (CVD) [13] and CVD oxide [23] on 4H-SiC, exhibit high dielectric reliability compared with thermal oxide. The MIS structure formed by  $\text{SiN}_x/\text{SiO}_2$  deposition, followed by  $\text{N}_2\text{O}$



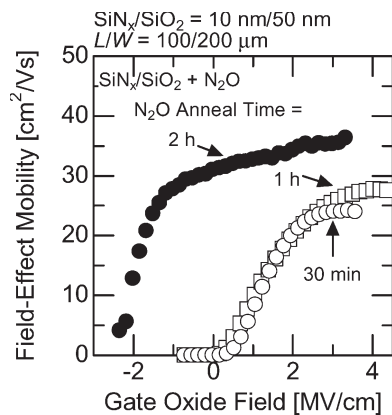


Fig. 7. Field-effect mobility of stack-gate MISFETs annealed in  $\text{N}_2\text{O}$ . The open circles, open squares, and closed circles correspond to the MISFETs annealed for 30 min (EOT = 56 nm), 1 h (57 nm), and 2 h (60 nm), respectively. These MISFETs have a deposited  $\text{SiN}_x/\text{SiO}_2$  thickness of 10 nm/50 nm.

annealing, may be one of the attractive approaches to improve the interface and dielectric characteristics.

Fig. 7 exhibits the field-effect mobility of MISFETs with  $\text{N}_2\text{O}$ -annealed  $\text{SiN}_x/\text{SiO}_2$  stack-gate structure on the (0001)Si face. Open circles, open squares, and closed circles correspond to the MISFETs annealed for 30 min, 1 h, and 2 h, respectively. The horizontal axis of Fig. 7 is the gate oxide field, which is defined as  $V_G/\text{EOT}$ . The field-effect mobility increases with extending  $\text{N}_2\text{O}$ -annealing time. The increase of field-effect mobility can be correlated with the reduction of interface trap density, as shown in Fig. 5. As predicted from its low interface trap density, a high channel mobility over  $30 \text{ cm}^2/\text{V} \cdot \text{s}$  was obtained when the  $\text{N}_2\text{O}$ -annealing time was 2 h. However, the MISFET annealed for 2 h shows a considerably shifted threshold voltage of  $-15 \text{ V}$ , which agrees with the large negative shift of the flat-band voltage obtained in the MIS capacitor shown in Fig. 4(b).

In the stack-gate MIS structures, the  $\text{SiN}_x$  layer is oxidized during  $\text{N}_2\text{O}$  annealing, and a portion of the  $\text{SiN}_x$  layer is converted to the  $\text{SiO}_x\text{N}_y$  layer, as shown in Fig. 3. Then, the MIS structure is changed from a  $\text{SiC}/\text{SiN}_x/\text{SiO}_2$  stack-gate structure to a  $\text{SiC}/\text{thin-SiN}_x/\text{SiO}_x\text{N}_y/\text{SiO}_2$  one. The influence of traps inside the  $\text{SiN}_x$  layer may be decreased by thinning the residual  $\text{SiN}_x$  layer. Thus, the lower interface trap density may be obtained by extending the  $\text{N}_2\text{O}$ -annealing time. In the MIS structure annealed in  $\text{N}_2\text{O}$  for 2 h, the  $\text{SiN}_x$  layer may be completely oxidized and converted to the  $\text{SiO}_x\text{N}_y$  layer, and the stack-gate structure becomes the  $\text{SiC}/\text{SiO}_x\text{N}_y/\text{SiO}_2$  structure, in which traps inside the  $\text{SiN}_x$  film disappeared, leading to the improvement of interface characteristics. The  $\text{SiO}_x\text{N}_y$  layer directly deposited on SiC by PECVD, followed by NO annealing, has already been investigated for the gate insulator of 4H-SiC MOS devices [24]. Compared with the previous report, the interface characteristics was significantly improved in the MIS structure, with the  $\text{SiO}_x\text{N}_y$  layer formed by oxidizing the  $\text{SiN}_x$  layer in this study. However, the stack-gate MIS structure annealed in  $\text{N}_2\text{O}$  for 2 h exhibits a large negative shift of the threshold voltage. Although the origin of this negative shift of the threshold voltage is unclear, a large positive charge should

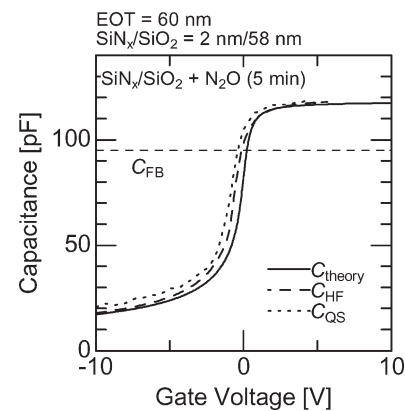


Fig. 8.  $C$ - $V$  characteristics for the stack-gate MIS capacitor with a thin  $\text{SiN}_x$  thickness of 2 nm, followed by  $\text{N}_2\text{O}$  annealing for 5 min. The solid, dashed, and dotted lines denote the theoretical characteristics, high-frequency characteristics, and quasi-static characteristics, respectively.

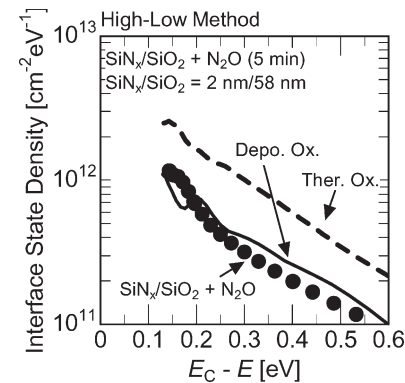


Fig. 9. Interface trap density for the  $\text{N}_2\text{O}$ -annealed stack-gate MIS capacitor with a  $\text{SiN}_x/\text{SiO}_2$  thickness of 2 nm/58 nm. The closed circles denote the stack-gate MIS capacitor. The dashed line denotes the MOS capacitor with thermal oxide, and the solid line denotes that with deposited oxide.

exist in the  $\text{SiO}_x\text{N}_y$  or at the  $\text{SiO}_x\text{N}_y/\text{SiC}$  interface [25]. In the case of the MIS capacitor, which was annealed for 1 h or shorter, it is possible that the negative charge (electrons) trapped at the interface traps compensates the positive charge located in the  $\text{SiO}_x\text{N}_y$  or at the  $\text{SiO}_x\text{N}_y/\text{SiC}$  interface. The MIS capacitor annealed for 2 h exhibits low interface trap density, and the negative charge captured at the interface traps is negligible, leading to a large negative shift of the flat-band voltage because of a large number of positive charges near the interface.

In order to reduce the large negative shift (positive charge), the initial thickness of the deposited  $\text{SiN}_x$  layer was decreased to 2 nm. The authors fabricated the stack-gate MIS capacitors and MISFETs, followed by  $\text{N}_2\text{O}$  annealing for 5 min. In order to completely oxidize the  $\text{SiN}_x$  layer, the short  $\text{N}_2\text{O}$ -annealing time was selected because of the very thin  $\text{SiN}_x$  layer. The optimum  $\text{N}_2\text{O}$ -annealing time depends on the initial- $\text{SiN}_x$  layer thickness (a thinner initial- $\text{SiN}_x$  layer needs a shorter  $\text{N}_2\text{O}$ -annealing time). The  $C$ - $V$  curves for the MIS capacitor with a 2-nm-thick initial- $\text{SiN}_x$  layer are shown in Fig. 8. The large negative shift of the flat-band voltage was not observed, and the flat-band voltage shift and effective fixed charge are very small, i.e.,  $-0.3 \text{ V}$  and  $1.2 \times 10^{11} \text{ cm}^{-2}$ , respectively. Fig. 9 represents the density of the interface traps for the stack-gate

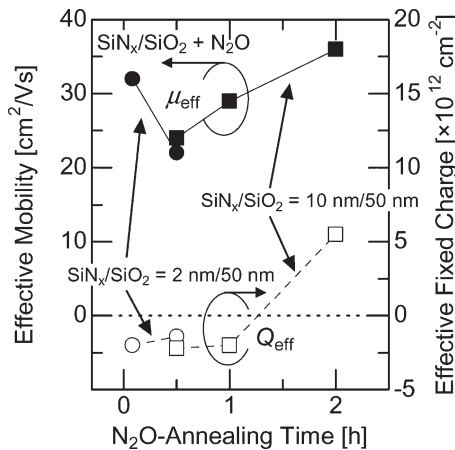


Fig. 10. N<sub>2</sub>O-annealing time dependence of effective mobility at the gate oxide field of 3 MV/cm and effective fixed charge calculated from the difference between the threshold voltages theoretically and experimentally obtained. The closed and open symbols mean the channel mobility and effective fixed charge, respectively. The circles denote the MISFETs with a SiN<sub>x</sub>/SiO<sub>2</sub> thickness of 2 nm/50 nm, and the squares denote those with a SiN<sub>x</sub>/SiO<sub>2</sub> thickness of 10 nm/50 nm.

MIS capacitor with the thin SiN<sub>x</sub> layer. Although the interface trap density for the MIS capacitor with a SiN<sub>x</sub> thickness of 2 nm is higher than  $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ , as shown by the closed circles in Fig. 5, it is still significantly lower than that for the MOS capacitor, with the thermal oxide grown in N<sub>2</sub>O. Compared with the deposited oxide, followed by N<sub>2</sub>O annealing, the stack-gate structure with the thin SiN<sub>x</sub> layer shows a slightly low density of the interface trap in the deep energy region.

Fig. 10 shows the N<sub>2</sub>O-annealing time dependence of effective channel mobility  $\mu_{\text{eff}}$  at the gate oxide field of 3 MV/cm and effective fixed charge  $Q_{\text{eff}}$  calculated from the difference between the theoretical and experimental threshold voltages. The MISFETs have a SiN<sub>x</sub>/SiO<sub>2</sub> thickness of 2 nm/50 nm or 10 nm/50 nm. In the case of a SiN<sub>x</sub> thickness of 10 nm, the effective mobility is increased by increasing the N<sub>2</sub>O-annealing time, whereas the mobility decreases with increasing N<sub>2</sub>O-annealing time in the MIS capacitor with a thin SiN<sub>x</sub> thickness of 2 nm. In the MIS structures with the thin-SiN<sub>x</sub> layer (2 nm), the time to completely oxidize the SiN<sub>x</sub> layer is shorter than that for the MIS structures with a SiN<sub>x</sub> thickness of 10 nm. Thus, the optimum N<sub>2</sub>O-annealing time may be shorter.

Fig. 11 shows the subthreshold characteristics ( $\log I_D - V_G/\text{EOT}$  characteristics) and the gate characteristics ( $I_D - V_G/\text{EOT}$  characteristics), and the field-effect mobility calculated from the gate characteristics is represented in Fig. 12, where the mobility of MOSFETs with thermal oxide and deposited oxide is also shown. The MISFET on the 4H-SiC (0001)Si face has a SiN<sub>x</sub>/SiO<sub>2</sub> thickness of 2 nm/50 nm annealed for 5 min. The authors have also fabricated the MISFETs on the 4H-SiC (0001)C face with an acceptor concentration of  $6 \times 10^{15} \text{ cm}^{-3}$ . In the C-face MISFET, the gate insulator was a SiN<sub>x</sub>/SiO<sub>2</sub> (2 nm/50 nm) stack structure annealed for 5 min, which is the same as that in the Si-face MISFET shown in Figs. 11 and 12. The threshold voltage obtained from the extrapolation of gate characteristics is 5.3 V for the MISFET on the Si face and 2.7 V for that on the C face,

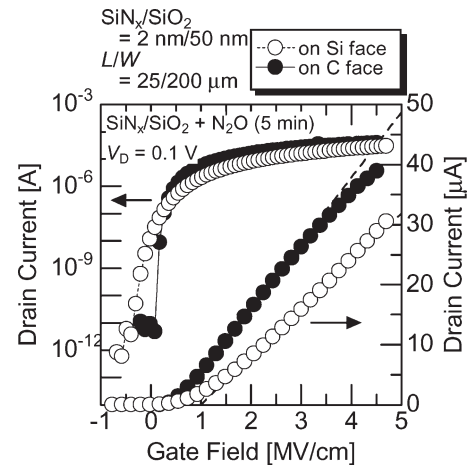


Fig. 11. Subthreshold and gate characteristics for stack-gate MISFETs annealed in N<sub>2</sub>O for 5 min with a SiN<sub>x</sub>/SiO<sub>2</sub> thickness of 2 nm/50 nm. The open and closed circles denote the MISFETs on the (0001)Si face and on the (0001)C face, respectively. (Both MISFETs have an EOT of 53 nm.)

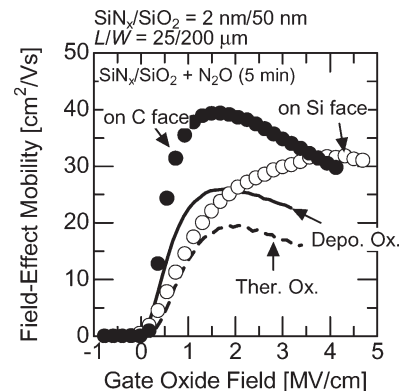


Fig. 12. Field-effect mobility for the stack-gate MISFETs annealed in N<sub>2</sub>O for 5 min with a SiN<sub>x</sub>/SiO<sub>2</sub> thickness of 2 nm/50 nm. The open and closed circles depict the mobility of MISFETs on the (0001)Si face and on the (0001)C face, respectively. These MISFETs have an EOT of 53 nm. The dashed line represents the mobility of MOSFETs with thermal oxide, and the solid line represents that with deposited oxide. The MOSFET with thermal oxide has an EOT of 97 nm, and that with deposited oxide has an EOT of 88 nm.

indicating the reduction of a large positive charge, as observed in Fig. 7. In Fig. 11, the MISFETs on the C face exhibits a steep slope in the subthreshold region of the  $\log I_D - V_G/\text{EOT}$  plots, and the subthreshold slope of the MISFETs on the C face was 182 mV/dec. On the other hand, the drain-current of the MISFETs on the Si face gradually increases from a gate oxide field of -0.5 MV/cm, and the subthreshold slope was 556 mV/dec. These results imply that the interface trap density of the C-face MISFETs is still lower than that of the Si-face MISFETs. While the MOSFETs with thermal oxide and deposited oxide show a channel mobility of 20 and 25  $\text{cm}^2/\text{V} \cdot \text{s}$ , respectively, a relatively high field-effect mobility of 32  $\text{cm}^2/\text{V} \cdot \text{s}$  is achieved in the stack-gate MISFETs on the (0001)Si face. This result indicates about 50% improvement in mobility. The channel mobility of MISFETs on the (0001)C face is 40  $\text{cm}^2/\text{V} \cdot \text{s}$ , suggesting a promise of the C face for MIS-based device application, as previously reported by using wet oxidation [9].

#### IV. CONCLUSION

In this study, SiN<sub>x</sub>/SiO<sub>2</sub> stack-gate structures deposited by PECVD and annealed in N<sub>2</sub>O were investigated for 4H-SiC MIS devices. The interface characteristics for the MIS capacitor with a SiN<sub>x</sub> thickness of 10 nm was significantly improved by extending the N<sub>2</sub>O-annealing time to 2 h. During N<sub>2</sub>O annealing, the deposited SiN<sub>x</sub> layer is oxidized, and the influence of traps inside the SiN<sub>x</sub> layer may be reduced. The MIS capacitor with a SiN<sub>x</sub>/SiO<sub>2</sub> thickness of 10 nm/50 nm, followed by N<sub>2</sub>O annealing for 2 h, exhibits a low interface trap density below  $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ . However, this MIS capacitor showed a large negative shift of the flat-band voltage, which indicates that positive charge exists in the oxidized SiN<sub>x</sub> layer (SiO<sub>x</sub>N<sub>y</sub> layer) or at the SiO<sub>x</sub>N<sub>y</sub>/SiC interface. Compared with thermal oxide, the dielectric properties were also improved in the stack-gate structure annealed in N<sub>2</sub>O. In order to suppress the large negative shift of the flat-band voltage, the initial thickness of the SiN<sub>x</sub> layer was decreased to 2 nm. The fabricated MISFETs with a SiN<sub>x</sub>/SiO<sub>2</sub> layer of 2 nm/50 nm annealed in N<sub>2</sub>O for 5 min demonstrated a high channel mobility of 32 cm<sup>2</sup>/V · s on the (0001)Si face and 40 cm<sup>2</sup>/V · s on the (000 $\bar{1}$ )C face, as well as “normally off” operation. The optimum N<sub>2</sub>O-annealing time for the MIS capacitor depends on the initial-SiN<sub>x</sub> thickness, because the time to completely oxidize the SiN<sub>x</sub> layer is different for these MIS capacitors. The deposited SiN<sub>x</sub>/SiO<sub>2</sub> stack-gate structure annealed in N<sub>2</sub>O ambient is one of the promising candidates for the gate insulator of 4H-SiC MIS devices.

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